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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,530	11/30/2001	Paul L. Master	QuickSilver Technology, I	6090

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GAMBURD LAW GROUP LLC
600 WEST JACKSON BLVD.
SUITE 625
CHICAGO, IL 60661

EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/997,530	MASTER ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-57,59-80,82-116,118-121 and 123-143* is/are pending in the application.

4a) Of the above claim(s) *6,58,81,117 and 122* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-57,59-80,82-116,118-121 and 123-143* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/05/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-5,7-57,59-80,82-116,118-121,123-143 are presented for examination. Claims 6, 58, 81, 117, 122 have been canceled. T.D. on 12/04/06 has been received.

2. New grounds of rejection have been applied to claims 41,42, 63, 70-72,78,79,84, 129,130,131,139 in response to newly amended features. However, rejections to claims 1-5,7-57,59-80,82-116,118-121,123-143 have been maintained and incorporated by reference the last Office action on 06/05/06 with claims 130,131,139 now being rejected under as being anticipated by Wise (5,768,561). Webb (4,760,525) is a newly cited art, and all other references have been cited on record.

3. The response filed on 12/04/06 has been fully considered but is not persuasive.

4. In the remarks, applicant argued that :

a) no packet routing in Baxter;

b) nested or multi-tiered interconnection network structure and corresponding configurability at multiple levels as illustrated in fig.4, page 14,11.3-19 is disclosed by prior art;

c) selective routing of configuration by one part of the interconnection network provides a configuration used by another part of the network is not being disclosed by prior art;

d) claim 94 recites an interconnection network for configuring computational elements in response to configuration information with routing elements that routs addressed data packets.

e) Lee's cellular phone is not relevant to adaptive, configurable or reconfigurable computing architectures and , not pertinent to present invention;

f) Cohen is not concerning configurable or adaptive computing .;

g) none of the prior art disclosed elements: an interconnection network comprising both routing elements and switching elements; using routing elements for configuration; different mixes or combinations of different computational elements forming independently configurable groups; and "self-routing" of data and configuration.

5. As to a) above, Baxter clearly taught transfer of data as packet-based messages (see col.32, lines 29-33).

6. As to b) , nested or multi-tiered interconnection network structure is not being claimed. applicant is reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)).

7. As to c), wise taught selective routing of configuration by one part (y[7,6] at input) of the interconnection network [common box] provides a configuration used by another part (see output at x[2,5] of the network.

8. As to d), Wise also directed to the routing elements that routs addressed data packets or the frames (see the frame point generated as address in col.6, lines 37-46) .

As to e), Lee taught upon occurrence determined by software, certain states can be entered into transitions, such as the standby, suspend, and awaken, (see col.11, lines 8-22). Therefore, Lee 's system is configurable and adaptive.

9. As to f) Cohen taught his system was intended to be practiced to assign electronic identifiers to facsimile machines, telephones, computers which were connected to data network (see col.2, lines 41-55). Therefore, Cohen is configurable and adaptive.

10. As to g), Wise taught an interconnection network (see the common box in fig.137) comprising both routing elements (see each path) and switching elements (see 2-input mux switch in fig.137); (2) using routing elements for configuration (see each of the routing elements such as adder, subtractor, multiplier) ; different mixes or combinations of different computational elements forming independently configurable groups (see reconfigurable path adder, carry subtractor, and subtractor, see also the reconfigurable path adder, carry adder, and subtractor in fig.137) .

As to the "self-routing" of data and configuration, no shelf routing has been reflected in to the claim. applicant is reminded that unclaimed features cannot be used to overcome

the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)).

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claim 129 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 24 of copending Application No. No. US 2006/0031660. Although the conflicting claims are not identical, they are not patentably distinct from each other because although claim 24 did not recite the first level of interconnection network adapted to selectively transfer data in response to the first configuration between the selected computational elements and the second level of the interconnection network to transfer data to the selected computational element and to transfer configuration information to the first level of the interconnection network as claim 129, the claim 24 also recites the interconnection network selectively route the configuration information and operand data to the plural fixed and differing computational elements and further configured to plurality of fixed and differing computational elements for at least one functional mode of a plurality of functional modes in response to the configuration information fixed and different computational elements (see claim24, lines 5-10). It would have been obvious to one of ordinary skill in the art to use a first level of interconnection network and second level of interconnection network as claimed because one of ordinary skill in the art should be able to recognize the data and configuration information could be selectively routed between the plural fixed and differing computational elements at a given bus interface, with was a first level of interconnection, and also could be selectively routed the bus interface itself in addition to a selected computational element, which was a second group or level of interconnection.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

12. Claims 32 , 41,42,63,70-72,78,79,84 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

13. As to the newly amended claims 32,63,

14. Claims 32, 63 now recite at least a method for adaptive configuration of an integrated circuit . However, the detailed structure of the integrated circuit is not being recited in to the claim body. Furthermore, the structural relation among the computational elements is unclear. Therefore, the integrated circuit and the computations elements are read as a general arrangement of the units. As to the use of the- routing elements, selectively routing data and the first subset of configuration information through the interconnection network to the first plurality of computational elements and selectively routing data and the second subset of configuration information through the interconnection network to the second plurality of computational elements to provide a selected operating mode of a plurality of operating modes. The configuration information and the selected operating modes are not the circuit itself.

The practical application of the selectively routing the configuration information and data is unclear. The focus is not on the step taken to achieve a final result which is useful, tangible, and concrete, but rather a final result achieved which is useful, tangible, and concrete. No final result of selectively routing and switching the data and configuration information can be found. Therefore, it is directed to non-statutory subject matter.

15. Furthermore, Claims 32,63 are not limited to tangible embodiments. In view of Applicant's disclosure, specification page 7 , lines 1-3,15,31, the adaptive configuration of an integrated circuit is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., [wireless base station]) and intangible embodiments (e.g., [wireless link] [air interface]). See also page 9. line 31 [wireless interface], page 27, line 10 [download through other medium], page 27, lines 29,30 [wireless download]. As such, the claim is not limited to statutory subject matter and is therefore non-statutory. The invention is not restricted into the hardware. For example, the receiving and transmitting the configuration information and the routing of the data through the interconnect network could be done over the air interface, for example the wireless download, therefore, it is not concrete and tangible. The downloaded configuration information can be in the form of frequency waves transmitted in the air space, therefore, it is directed to a non-statutory subject matter.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 63 is rejected under 35 U.S.C. 102(b) as being anticipated by Webb (4,760,525).

16. As to claim 63, Webb (4,760,525) taught at least :

a) transmitting a first set of configuration information (see DATA2-DATA7 in fig.6) , the first set of configuration information comprising a first subset of configuration information (DATA2, DATA3, DATA2, DATA4) and a second subset of configuration information (DATA5, DATA3, DATA6, DATA7);

wherein when the first set of configuration information is received;

using the routing elements (601,602), selectively routing data and the first subset of configuration information through the interconnection network (see fig.6) to the first plurality of computational elements (see ALU1 ALU2) and selectively routing data (see DATA) and the second subset of configuration information through the interconnection network to the second plurality of computational elements (ALU4 ALU3) to provide a selected operating mode of a plurality of operating modes; and

using the switching elements (661,662) , configuring through the second level of the an interconnection network the first plurality of fixed and differing computational elements for a first functional mode (see the selection output odes RE1 RF and RG1 at MXB1

and MXB2 in fig.6) of a plurality of functional modes in response to the first subset of configuration information (see the selected input data at 661 and 662) , and a second plurality of fixed and differing computational elements (ALU4 ALU3) for a second different functional mode of the plurality of functional modes (see output modes at RE1 RF and RG1 at MXB3 and MXB4) in response to the second subset of configuration information (see input data at 663,664).

17. Claims 1-5,7-15, 17, 18, 20,21,23,27-46, 48,49,,51-58, 62-76, 78-85, 89-99,101-128 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Baxter (5,794,062).

18. As to the newly amended feature in claim 1, Wise also taught a plurality of routing elements (see buses in common block in fig.137) adapted to provide a selected operating mode (see the Y inputs in fig.137) of a plurality of operating modes by selectively routing data and a first and second subsets of configuration information (see c1 and c3) to the corresponding first or second pluralities of computational elements (see carry adder and carry subtractor) , and a second level of the interconnection network (see 2-input mux latch, see fig.137) comprising a plurality of switching elements (see 2-input mux latch) adapted to configure the plurality of heterogeneous computational elements (see carry adder and subtractor) for a first functional mode x[3,4] of a plurality of functional modes, in response to the first subset of configuration information (see configuration carry-save multiplier, carry save adder, carry save

subtractor in the common block), and the interconnection network further operative to reconfigure the plurality of heterogeneous computational elements for a second functional mode (x[2,5]) of the plurality of functional modes, in response to the second sub set of configuration information (see carry save multiplier, carry save subtractor, carry save subtractor), the first functional mode (x[3,4]) being different than the second functional mode (x[2,5]);

19. As to newly amended claims 32, 63, Wise also taught the use of the- routing elements (see each path in fig.137) , selectively routing data (e.g. see input at Y [3,2] Y[7,6]) and the first subset of configuration information (see adder and carry subtractor) through the interconnection network (see common box 137) to the first plurality of computational elements (see X[2,5], x[3,4] and selectively routing data and the second subset of configuration information (see the adder, adder) through the interconnection network (common box) to the second plurality of computational elements X[1,6], x[0,7] to provide a selected operating mode (adder) of a plurality of operating modes(see combined groups of adders and subtractors and multipliers). As to the fixed and different computational elements at first level, see (X[0,7] X[1,6]), and the second level X[3,4],X[2,5].

20. As to newly amended claim 89, Wise also taught :

a) a plurality of configurable matrices (y[1,0] x[0,7], y[5,4], x[1,6]), at least two configurable matrices of the plurality of configurable matrices each comprising a first interconnection network(see each line path in common box in fig.137) and different pluralities of fixed and differing computational elements (see adder, multiplier, dummy adder/subtractor) , each corresponding plurality of fixed and differing computational elements (multiplier, dummy adder, adder) coupled to the corresponding first interconnect network (top line of the common box in fig.137) and configurable for a corresponding functional mode (Y[1,0]Y[5,4]) through configuration of a plurality of input and output connections (see inputs at Y nodes) by the corresponding first interconnection network in response to the configuration information (see corresponding configuration information in Key 137); and

a second matrix interconnection network (y[3,2] x[3,4] , y[7,6]x[2,5] , lines 3,4 of the common block) coupled to the plurality of configurable matrices, the matrix interconnection network adapted to configure the plurality of configurable matrices for a selected operating mode (Y) of a plurality of operating modes (functions at Y nodes) by selectively transferring data (see constants) and configuration information (see configurable adder and subtractor path in fig.137) to the plurality of configurable matrices.

21. As to claim 91, Wise also taught (see fig.137) :

a) first and second plurality to heterogeneous computational elements (see resolving adder/subtractor at lines y[1,0] x[0,7] and y[5,4], x[1,6] of fig.137);

b) a plurality of interconnection networks (common block line 1,2) coupled to the first and second plurality of heterogeneous computational elements, a first interconnection network (line 1 common block) of the plurality of interconnection networks (lines 1,2 of common block) comprising a plurality of routing elements (see each connection point of line 1) capable of differentially routing data and configuration information to the first] and second pluralities of heterogeneous computational elements (see adders and subtractors at a given line), a second interconnection network (see 2-inpout mux switches) in fig. 137) of the plurality of interconnection networks comprising a first plurality of switching elements (see top two 2-input mux latches) capable of configuring the first plurality of heterogeneous computational elements for a first functional modes (see anyone of the Y functions) of a plurality of functional modes in response to the first configuration information (see constant and multiplier at the top line) , and a third interconnection network (see bottom two 2-input mux latches) of the plurality of interconnection networks comprising second plurality of switching elements (2-input mux latches) capable of configuring the second plurality of heterogeneous computational elements for a second different functional mode (any of y[3,2] y[7,6]) of the plurality of functional modes in response to the second configuration information (see output of the adder).

As to newly amended claim 93, Wise also taught :

a) a first interconnection network (see Y and X sides to the common block in fig.137) coupled to the plurality of computational elements (see adders and subtractors) , the interconnection network comprising a plurality switching elements (see 2-input mux

latches) of capable of configuring the plurality of computational elements for a plurality of functional modes (see Y functional modes) in response to the configuration information (see multiplier and multiplier output) by selectively switching input (see input at carry-save multiplier) and output (see output at carry-save multiplier) connections between selected computational elements of the plurality of computational elements and

b) a second interconnection network (see common block in fig.137) coupled to an interface (see input/output common box) , to the plurality of computational elements (se adders, subtractors, multipliers) and to the first interconnection network, the second interconnection network comprising a plurality of routing elements (see each path in the common block) capable of providing a selected functional mode of the plurality of functional modes (see Y function modes) in response to the configuration information by selectively routing data packets (see constants) to selected computational elements of the plurality of computational elements and selectively routing configuration information packets to the first interconnection network (see output at common block).

22. As top newly amended claims 94,101, see discussions in Paragraph 4 d) above.

23. Claims 16,19, 22, 24-26, 47,50, 77, 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Baxter (5,794,062) in view of Lee et al. (5,873,045).

24. Claims 59-61, 86-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Baxter (5,794,062) in view of Cohen et al. (6,005,943).

25. Claim 129,130,131 are rejected under 35 U.S.C. 102(b) as being anticipated by Wise (5,768,561).

As to newly amended claim 129, 130, Wise also taught :

a) a first plurality of fixed and differing computational elements forming a first configurable architecture (see adders, subtractors of the bottom two lines in fig.137);

b) an interconnection network (see fig.137) coupled to the first plurality of computational elements, a first level of the interconnection network (see the 2-input mux latches) adapted to selectively transfer data, in response to first configuration information (see Y), between selected computational elements of the first plurality of computational elements, and a second level of the interconnection network (see Y lines and common block lines) adapted to transfer data (see Y input) selectively to a selected computational element of the first plurality of computational elements and to transfer the first configuration information (see how the constant c1 and c3 being transferred to other computational elements) selectively to the first level of the interconnection network.

26. As to newly amended claim 131, Wise also taught :

a) a second plurality of fixed and differing computational elements forming a second, different configurable architecture (see the adder and subtractor of the top two lines of fig.137); and

b) a corresponding first level of the interconnection network (see the 2-input mux latches) coupled to the second plurality of computational elements, the corresponding first level of the interconnection network adapted to selectively transfer data (see adder and multiplier output before 2-input mux latch), in response to second configuration information (Y input), between selected computational elements of the second plurality of computational elements; wherein the second level (Y lines and common block lines) of the interconnection network is further adapted to transfer data selectively to the second plurality of computational elements (see transfer lines from line 1 to line 2) and to transfer the second configuration information selectively to the corresponding first level of the interconnection network (see Y[1,0] on line 1).

27. Claim 132-143 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Baxter (5,794,062).

28. As to newly amended claim 139, Wise also included routing elements (see data lines between Y and X) and switching elements (see 2-input mux latches in fig.137).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP